Audio data converters and miscellaneous digital audio ICs designer's guide

SECTION 1 - INTRODUCTION

This guide supplements Data Handbooks IC01a and IC01b (Semiconductors for radio and audio systems) to provide a simple means of evaluating the features and performance of the extensive range of Philips' audio data converters and dedicated signal processing ICs.

Philips scored a first in 1987 by developing the bitstream data conversion technique which converts binary samples of an analog audio signal into a 1-bit code using oversampling, noise shaping and pulse density modulation (PDM). Compared with multi-bit DACs, our bitstream conversion DACs have improved small-signal linearity, no "glitches" and no crossover distortion effects. We have a wide range of DACs of this type plus a digital filter for, noise shaping, digital filtering and post filtering requirements of all classes of digital audio equipment.

We also have four bitstream ADCs, and a wide selection of conventional 16-bit DACs. For portable applications, where small dimensions and low power consumption are prerequisites, we have a comprehensive range of very low power continuous calibration DACs (CC-DACs).

Our range of audio data conversion ICs is completed with a quadruple sign-magnitude filter DAC (QDAC) for front and rear stereo in car applications, and a bitstream/continuous-calibration ADC/DAC.

Other important Philips products for digital audio systems include a digital input/output circuit (DAIO), a general digital input circuit (GDIN), a digital audio processing IC (DAPIC), a headphone driver and MPEG devices.

Naturally, Philips Semiconductors support for audio data converters and dedicated signal processing ICs doesn't end with the supply of this extensive range of ICs described in this guide. We also offer access to the wide-ranging expertise of our international applications laboratories to assist with your hardware/software designs for specific applications. Should you require further information, please contact your nearest Philips National Organisation; their addresses are on the back cover of this guide.

Data transfer in digital audio systems

Exchanging audio data between ICs in a digital audio system is often hampered because each manufacturer incorporates his own dedicated interface. This makes it difficult to use ICs from different manufacturers in the same system. For maximum design flexibility, a vital requirement for both the equipment manufacturer and the IC manufacturer is the availability of standardized communication structures. To meet this requirement, Philips have developed the Inter-IC Sound (I^2S) interface.

The I^2S-interface

The I^2S-interface is a serial link dedicated to data transfer between ICs in digital audio systems.

Signals other than audio data, such as sub-coding and control, are transferred separately. To minimize the number of pins, and to keep the wiring simple, I^2S is a serial interface consisting of 3 lines; serial data (SD) for two time-division multiplexed channels, left/right channel word select (WS), and serial clock (SCL).

The transmitter and receiver have the same clock signal for data transmission. In a simple two-IC system, the master (transmitter or receiver), must generate the bit clock and word select signal, and the transmitter generates the data.

Table 1-1 General documentation relating to audio data converters and miscellaneous digital audio ICs

Title	Ordering code	Type of publication
Semiconductors for radio and audio systems - 80C31 to TDA1381	9398 652 61011	Data Handbook IC01a
Semiconductors for radio and audio systems - TDA1386T to TSA6060	9398 652 62011	Data Handbook IC01b
The I^2C-bus and how to use it (including specifications)	9398 393 40011	Brochure
Design-in guide: Compact disc player ICs and systems	9398 706 91011	Design-in guide

SECTION 2 - STEREO DIGITAL AUDIO DATA CONVERTERS

Essential functions in digital audio equipment are the analog-to-digital conversion (ADC), and the digital-to-analog conversion (DAC). These signal processing stages play a major and critical role by converting audio signals into 16-bit sound data words (ADC), and by converting 16-bit sound data words which have been numerically decoded and filtered, into analog waveforms which can be made audible (DAC).

Philips have developed an extensive range of stereo data converters using four different conversion techniques to meet the diverse requirements of the digital audio market:

- •Bitstream conversion stereo ADCs and DACs for top-class audio performance
- •Conventional 16-bit stereo DACs
- •Continuous calibration stereo DACs which are the world's smallest converters with the lowest power consumption
- •Stereo filter-DACs that use bitstream conversion for small signals, and the continuous calibration technique for large signals
- •A quadruple sign-magnitude filter-DAC for 4-channel (front and rear stereo) digital audio applications in cars
- •A combined stereo bitstream ADC with digital filter and bitstream/continuous calibration DAC.

A survey of our extensive range of stereo audio DACs is given in Table 2-3.

The bitstream conversion technique

The bitstream digital-to-analog conversion technique, developed by Philips, converts binary samples (e.g. 16-bit words) into a 1-bit code representing two levels (0 or 1) using oversampling, noise shaping and pulse density modulation (PDM). This code is then converted into an analog form that closely resembles the original signal by a switched-capacitor conversion technique. Because bitstream converters process the signal in the digital domain, they have the following advantages over conventional multi-bit converters:

- •Considerable improvement of small-signal linearity
- •Absence of glitches
- •Complete elimination of cross-over effects.

Bitstream conversion ADCs (Table 2-13)

Philips offer two bitstream conversion ADCs. Both are for use in digital audio playback systems such as digital amplifiers, CD-recordable and Digital Compact Cassette (DCC). Each device consists of an input buffer for pre-scaling and anti-aliasing, a 3rd-order Sigma-Delta modulator and decimation filters for anti-aliasing suppression and low in-band ripple. The choice of two ADCs allows selection of high or economy performance in accordance with application requirements.

Top-grade bitstream conversion DAC with separate bitstream digital filter (Table 2-4)

Our top-grade bitstream DAC is a BiMOS circuit without noise shaping, digital filtering or post filtering. It is intended for use in combination with our advanced bitstream digital filter. This results in optimum performance by reducing crosstalk between the analog and digital sections of the circuitry, extending the dynamic range, and increasing the signal-to-noise ratio. Furthermore, the BiMOS process used for the DAC allows MOS transistors to be used for the digital logic and drivers, and bipolar transistors to be used to achieve low noise analog circuitry. This optimizes speed and reduces digital noise. Other precautions taken in the DAC design to ensure maximum immunity to crosstalk are:

- •Fully separated L and R channels
- •Separate supply lines for the analog and digital sections.

Our advanced oversampling digital filter for use with the top-grade bitstream conversion DAC uses bitstream conversion technology. This two chip approach is ideal for premium performance digital audio applications. Audio data can be applied to the input of the digital filter in I^2S, or Sony (“S”) 16-, 18- or 20-bit format. A high quality bitstream is produced for application to the input of the DAC, resulting in the highest audio performance presently available in the electronics industry. This is largely due to thehighly-accurate audio data processing structure of the filter which includes 8x oversampling, digital filtering and up to 4th-order noise shaping.

These two ICs achieve a high degree of versatility by providing a multitude of easily accessed functional features. Error concealment functions, audio peak data, and an advanced patented digital fade function are all accessible through a simple

microprocessor command interface which also provides access to various integrated system settings and functions.

Sixteen-bit DACs

Our range of bipolar 16-bit DACs for audio applications comprises three high-performance DACs, three economy DACs and a low-noise DAC.

High-performance 16-bit DACs (Table 2-6)

In these DACs, the ten lowest bits are derived from a reference current by means of a passive 10-bit current divider based on emitter scaling. The six highest bits are constructed by dynamic element matching (DEM), a technique patented by Philips. rom an internal oscillator. After time-averaging, the resulting four output currents are very closely matched.

Two of the four output currents generated in the first DEM stage are added to form the largest (MSB = bit 16) bit current. The third output current forms thesecond largest (MSB _ 1 = bit 15) bit current. The fourth output current is fed into the next DEM stage to construct bits 13 and 14. Similarly, the fourth output current from the second DEM stage is fed into the final DEM stage to construct bits 11 and 12. The fourth output current from the final DEM stage is fed to the passive 10-bit current divider to construct the 10 LSBs (bits 1 to 10). In this manner, all sixteen bit currents are derived from the same current reference.

Economy and low-noise 16-bit DACs (Table 2-7)

Our economy, cost-efficient 16-bit DACs are characterized by their simple application. All that's needed is a single 5 V supply and one supply decoupling capacitor.

The serial data input is shifted-in at the TTL-compatible interface. Two address pointers correctlyposition each data bit in the left and right input registers, and the left and right 16-bit words are simultaneously latched to the associated output registers which each drive symmetrical bit switches. Passive current dividers generate the 16 bit currents switched by the symmetrical bit switches. A low-noise current source drives left and right 11-bit passive dividers, one current from each of which is fed into an associated 5-bit passive divider to achieve a dynamic range of 16 bits. An adjustable bias current, derived from the current through the V_{REF} pin, is added to the output currents. V_{REF} can also be used as a reference for op-amps at the analog outputs.

Our low-noise 16-bit DAC is an improved version of our economy DACs with a higher signal to noise ratio and lower harmonic distortion with small signals (at _60 dB). Furthermore, it has a full-scale output current of 3 mA ±10% compared with 2.3 mA ±15% for the economy DACs.

Continuous calibration DACs (CC-DACs) and filter-DACs

As shown in Fig.2-1, DEM uses matched resistors to divide a

Continuous calibration is an innovative data conversion technique patented by Philips and implemented in our new range of CMOS CC-DACs for cost-effective D to A conversion in portable equipment.

The technique of continuous calibration is based on the principle of storing charges on the gate-source capacitance of internal CMOS transistors. Thischarge storage principle allows the largest bit currents to be generated repeatedly from a single reference current. Because only one internal reference source is required, these coarse bit currents are extremely closely matched and immune to ageing, temperature and process variations or matching.

The basic operation of a CC-DAC (Fig.2-2) consists of continuous cycles of calibrating the drain current of CMOS transistors to a reference current, and then extracting an exact duplicate of the reference current from the drain. During calibration, the MOS transistor is connected as a diode in parallel with its gate-source capacitance by linking its drain and gate. The drain of this diode-connected transistor is connected to a constant reference current source so that the intrinsic gate-source capacitance charges to a voltage determined by the characteristics of the transistor. The drain-gate link and reference current source are then disconnected and, since the charge on the intrinsic gate-source capacitance of the transistor is preserved, an exact duplicate of the reference current is available as an output at the drain.

Fig.2-1 Structure of a high-performance 16-bit DAC. The binary-weighted current network derives the 16 most-significant bit currents from the reference current source. The 10 least-significant bit currents originate from the passive divider. The 6 most-significant bit currents are generated by time-averaging in the 3 Dynamic Element Matching (DEM) sections

Fig.2-2 Principle of continuous calibration (a) calibration (b) operation

CC-DACs use symmetrical offset decoding in which the bit switching is arranged so that the zero-crossing transition is performed by switching only the smallest currents. The intrinsic highly accurate coarse current, combined with the symmetrical offset principle, precludes any distortion at the zero-crossing or at any other small-signal transitions. CC-DACs are therefore capable of high-quality reproduction of low-level audio input signals.

Philips' CC-DACs are fabricated in a 1.0 µm CMOS process and feature extremely low power dissipation, small packages and simple application.

Our present range of CC-DACs for audio applications comprises a CC-DAC with current output, a relaxed-specification version, two CC-DACs with voltage output, and a third improved version which can handle 8x oversampled simultaneous input data streams.

We also have two continuous-calibration filter-DACs which each incorporate a cascaded 4-stage digital filter and noise shaping

CC-DACs with current output (Table 2-8)

In these two DACs, 32 current sources and one spare current source are continuously calibrated. The 32 current sources define the 5 MSBs. The spare current source is included to allow continuous converter operation. The output from one of the calibrated current sources is connected to an 11-bit binary current divider containing 2048 transistors which defines the 11 LSBs.

These DACs accept 16-bit serial data input words with left and right channel words time-division multiplexed. The MSB (bit 1) must always be first. With the Word Select (WS) input HIGH, input data are placed in the left input register; with it LOW, input data are placed in the right input register. The data in the input registers are simultaneously latched to the associated output registers which control the bit switches.

The only difference between these two DACs is that one of them has THD + noise at full-scale of 0.05%, and the other 0.005%. This makes the former eminently suitable for use in cost-efficient applications.

CC-DACs with voltage output (Table 2-9)

These are derivatives of the CC-DAC with current output. They include integrated I/V converters at their analog outputs. This produces a voltage output, thereby allowing the number of peripheral components to be reduced to one small decoupling capacitor.

The basic version of this type of DAC has a $4f_S$ oversampling data input format which is compatible with most currently used non-I^2S input formats (time-division multiplexed, two's complement, TTL).

An improved version can handle up to $8f_S$ oversampled data input streams which are compatible with most dual input serial data, two's complement, TTL input formats.

The final CC-DAC in this category is a low-noise version with selectable $4f_S/8f_S$ oversampled data input streams

Bitstream/CC filter-DACs (Table 2-10)

These filter-DACs feature a unique combination of bitstream and continuous calibration techniques. The DAC functions as a bitstream converter for low-level signals, and as a dynamic continuous calibration converter for large signals. This technique results in low power consumption, a small chip and simple application.

These DACs include up-sampling filtering and noise-shaping. The combination of high oversampling up to $16f_S$, second-order noise-shaping and continuous calibration ensures that only simple 1st-order analog post-filtering is required.

These DACs accept input in I^2S format or Japanese format with word lengths of 16, 18 and 20 bits. Four cascaded filters increase the oversampling rate to x16. A sample-and-hold function increases the oversampling rate in normal speed mode to x96 ($f_{sys} = 384f_S$) or x128 ($f_{sys} = 256f_S$) or to x48 ($f_{sys} = 256f_S$) or x64 ($f_{sys} = 384f_S$) . A 2nd-order noise shaper converts this oversampled data into a bitstream.

The DACs incorporate special data encoding. This ensures an extremely high signal-to-noise ratio, superior dynamic range, and immunity to process variations and component ageing.

Two on-chip operational amplifiers convert the DAC output currents into voltages. Externally-connected capacitors perform the required 1st-order post filtering. No further filtering is required.

The unique combination of bitstream and continuous-calibration techniques, together with a high degree of analog and digital integration, results in a single-filter DAC with 18-bit dynamic range, high linearity, and simple, low-cost application.

Quad sign-magnitude filter-DAC (Table 2-12)

This is a quadruple low-noise, wide dynamic range filter-DAC for use in car digital audio systems with front and rear stereo output. Each of the four channels

comprises an 8th-order IIR filter with up-sampling from $1f_S$ to $4f_S$ followed by a 1st-order noise shaper and a sign-magnitude DAC. The output current is converted into a voltage by an individual operational amplifier for each of the four channels.

Bitstream/CC ADC/DAC (Table 2-14)

This IC contains a two-channel (stereo) ADC, a two-channel DAC, reference circuits, analog I/O buffers (op-amps), digital

decimation and interpolation filters, and I/O interfaces. The ADCs are bitstream types with simultaneous sampling of both channels. The DACs are bitstream/CC types. The digital filter for the ADCs is a bit-serial IIR type with fairly linear phase response up to 15 kHz. A high-pass filter in the down-sampling path removes DC offsets. Overload detection facilitates automatic adjustment of recording level.

The digital up-sampling filter for the DACs is partly IIR, with almost linear phase response up to 15 kHz, and partly FIR. Switchable de-emphasis is included. Due to the bitstream/CC technique, the DACs only require 1st-order post filtering (one external capacitor) to satisfy the out-of-band suppression requirement.

Table 2-1 Documentation relating to stereo audio ADCs and DACs

Title	Ordering code	Type of publication
Bitstream conversion	9398 379 80011	Booklet
TDA1541A stereo 16-bit D to A converter for medium and high-end performance digital audio applications	9398 074 30011	Lab. report
Application and performance of the SAA7360 bitstream audio ADC	JRA/AN93001	Lab. report
Application and performance of the SAA7366 bitstream audio ADC	JRA/AN93003	Lab. report
Application and performance of TDA1545(T): continuous calibration audio DAC	NBA/AN9101	Application note
Single active stage 3rd-order I-to-V filtering for low-end current output DACs	NBA/AN9107	Application note
TDA1547 top-grade stereo bitstream digital-to-analog converter	NBA/AN9006	Application note
TDA1547 stereo top-performance bitstream digital-to-analog converter IC		Leaflet
Bitstream digital audio reconstruction system	NBA/AN9303	Application note
A printed-circuit board for the combination of TDA1307 bitstream digital filter and TDA1547 bitstream DAC	NBA/AN9305	Application note
Audio performance measurements on bitstream unicon I featuring TDA1315, TDA1307 and TDA1547	NBA/AN9307	Application note
A PCB for the TDA1305T digital filter and bitstream/continuous calibration DAC	NBA/AN9311	Application note
TDA1306T/TDA1386T noise shaping filter DAC	NBA/AN9312	Application note
Audio performance measurements on bitstream Unicon I featuring TDA1315, TDA1307 and TDA1547	NBA/AN9308	Application note
Supplement: Bitstream Unicon II digital audio converter	NBA/AN9310	Application note
Application of the TDA1546T, a bitstream continuous calibration DAC with digital filter and DSP features	NBA/AN9414	Application note
TDA1548T(Z): low-power, low-voltage headphone filter DAC	NBA/AN9507	Application note

Table 2-2 Main application areas of stereo audio converters

Type	Description	Home hi-fi	Portable hi-fi	Car	Multimedia
SAA7360 GP	high-performance bitstream ADC	–		–	
SAA7361 GP	premium-grade bitstream ADC	–		–	
SAA7366T	economy bitstream ADC	–		–	
SAA7367T	economy bitstream ADC	–		–	
TDA1305T (AT)	bitstream/CC filter-DAC	–	–	–	–
TDA1306T	CC filter-DAC	–	–	–	–
TDA1307	high-performance bitstream digital filter	–			
TDA1309H	low-voltage bitstream/CC ADC + DAC	–	–	–	
TDA1310A (AT)	continuous calibration DAC with current output	–	–	–	–
TDA1311A (AT)	continuous calibration DAC with voltage output	–	–	–	–
TDA1312A (AT)	continuous calibration DAC with voltage output	–	–	–	
TDA1313(T)	continuous calibration DAC with voltage output	–	–	–	

TDA1314T	quad sign-magnitude filter-DAC with voltage output	–	–	–	
TDA1386T	CC filter-DAC	–	–	–	
TDA1387T	continuous calibration DAC with current output	–	–	–	–
TDA1541A	high-performance 16-bit DAC	–			
TDA1541A /R1	high-performance 16-bit DAC	–			
TDA1541A /S1	single crown 16-bit DAC	–			
TDA1541A /S2	double crown 16-bit DAC	–			
TDA1543(T)	economy 16-bit DAC	–		–	
TDA1543A (AT)	economy 16-bit DAC	–		–	
TDA1545A (AT)	continuous calibration DAC with current output	–	–	–	–
TDA1546T	bitstream/CC filter-DAC + DSP features	–	–	–	
TDA1547	top-grade BiMOS bitstream DAC	–			
TDA1548T	low-voltage bitstream/CC filter-DAC + DSP features		–	–	
TDA1549(T)	bitstream/CC DAC	–	–	–	

	Type	Description	Over-sampling (x f_S)	Data input format	Typ. THD + N at 0 dB dB(%)	Typ. THD + N at −60 dB dB(%)	Typ. signal-to-noise ratio [4] (dB)	Typ. output voltage (or current) [6] V (mA)	Supply voltage (V)	Power (m
formance bitstream ADC			128	data output format: I^2S + two pseudo I^2S	_90(0.003)		102		5 ±10%	4
n-grade bitstream ADC			128	data output format: I^2S + two pseudo I^2S	_94(0.002)		102		5 ±10%	4
y bitstream ADC			128	data output format: I^2S + one pseudo I^2S	_88(0.004)		95		5 ±10%	3
y bitstream ADC			128	data output format: I^2S + one pseudo I^2S	_88(0.004)		95		5 ±10%	
n/CC filter-DAC			96	I^2S, "S", $1f_S$, up to 20-bit	_90(0.003)	_46(0.5)	108	1.5	3.4 to 5.5	
-DAC			4	I^2S, "S", $1f_S$, up to 20-bit	_70(0.032)	_42(0.8)	108	1.1	5 ±10%	
ge bitstream/CC	ADC + DAC	**ADC**		I^2S, "S", 16-bit, 18-bit output	_85(0.005)	_35(1.7)	95		2.7 to 4.0	
		DAC	256	I^2S, "S", 16-bit, 18-bit input	_90(0.003)	_44(0.6)	104	0.5		
us calibration DAC	with current output		1	"S", up to $4f_S$	_65(0.05)	_33(2.2)	95	(1.0)	3 to 5.5	
us calibration DAC	with voltage output		1	"S", up to $4f_S$	_68(0.04)	_33(2)	92	2.0	4 to 5.5	

o audio ADCs and DACs in type number sequence

Table 2-3b Survey of stereo audio DACs (ranked by typical THD + N at 0 dB performance per category)

us calibration DAC	with voltage output	1	"S", up to $8f_S$	_68(0.04)	_33(2)	92	2.0	4 to 5.5	
us calibration DAC	with voltage output	1	"S", up to $8f_S$	_88(0.004)	_38(1.3)	98	4.2	3 to 5.5	
gn-magnitude filter	-DAC with voltage output	4	2 x I^2S, $1f_S$, 18-bit with sign	_70(0.03)	_42(0.8)	110	2.0	5 ±5%	
-DAC		4	I^2S, "S", $1f_S$, up to 20-bit	_70(0.032)	_42(0.8)	108	1.1	5 ±10%	
us calibration DAC	with current output	1	I^2S, up to $4f_S$	_88(0.004)	_35(1.7)	98	(1.0)	3 to 5.5	
formance 16-bit DAC		1	I^2S, up to $8f_S$	_95(0.0018)	_42(0.79)	112	(4.0)	5 ±10%	7
formance 16-bit DAC		1	I^2S, up to $8f_S$	_95(0.0018)	_43(0.7)	112	(4.0)	5 ±10%	7
own 16-bit DAC		1	I^2S, up to $8f_S$	_95(0.001)	_47(0.4)	112	(4.0)	5 ±10%	7
crown 16-bit DAC		1	I^2S, up to $8f_S$	_97(0.002)	_47(0.4)	112	(4.0)	5 ±10%	7
y 16-bit DAC		1	I^2S, up to $4f_S$	_75(0.018)	_33(2.2)	96	(2.30)	3 to 8	2
y 16-bit DAC		1	"S", up to $4f_S$	_75(0.018)	_33(2.2)	96	(2.30)	3 to 8	2
us calibration DAC	with current output	1	"S", up to $4f_S$	_88(0.004)	_35(1.7)	101	(1.0)	3 to 5.5	
n/CC filter-DAC +	DSP features	96	I^2S, "S", $1f_S$, up to 20-bit	_88(0.004)	_44(0.6)	108	1.5	3.8 to 5.5	2
e BiMOS bitstream DAC		24	1-bit, $192f_S$	_101(0.0009)	_51(0.02)	113	1.0	5 ±10%	8
age bitstream/CC	filter-DAC + DSP features	96	I^2S, "S", $1f_S$, up to 20-bit	_85(0.005)	_35(1.8)	95	0.7	2.7 to 4	
n/CC DAC		24	"S", $4f_S$, 18-bit	_90(0.003)	_50(0.32)	110	1.5	3.8 to 5.5	

Notes: [1] measured with SAA7350 and 20-bit input; [2] includes digital filter; [3] high sound quality: dynamic r
[4] A-weighting; [5] includes I/V converter; [6] full-scale rms value.

	Type		Description	Over-sampling (x f_S)	Data input format	Typ. THD + N at 0 dB dB(%)	Typ. THD + N at −60 dB dB(%) [4]	Typ. signal-to-noise ratio dB (dB) [4]	S
Bitstream DAC									
1547[1]	top-grade BiMOS bitstream DAC			24	1-bit, $192f_S$	_101(0.0009)	_51(0.02)	113	
Bitstream/continuous calibration DACs									
1549(T)[5]	bitstream/CC DAC			24	"S", $4f_S$, 18-bit	_90(0.003)	_50(0.32)	110	
16-bit DACs									
1541A/S	double crown 16-bit DAC			1	I^2S, up to $8f_S$	_95(0.002)	_47(0.4)	112	
TDA1541A/S1[3]	single crown 16-bit DAC			1	I^2S, up to $8f_S$	_95(0.001)	_47(0.4)	112	
TDA1541A[3]	high-performance 16-bit DAC			1	I^2S, up to $8f_S$	_95(0.0018)	_42(0.79)	112	
TDA1541A/R1[3]	high-performance 16-bit DAC			1	I^2S, up to $8f_S$	_95(0.001)	_43(0.79)	112	
TDA1543(T)	economy 16-bit DAC			1	I^2S, up to $4f_S$	_75(0.018)	_33(2.2)	96	
TDA1543A(AT)	economy 16-bit DAC			1	"S", up to $4f_S$	_75(0.018)	_33(2.2)	96	
Continuous calibration DACs									

1313(T)[5]	continuous calibration DAC with voltage output			1	“S”, up to $8f_S$	_88(0.004)	_33(1.3)	98	
TDA1545A(AT)	continuous calibration	DAC with current output		1	“S”, up to $4f_S$	_88(0.004)	_35(1.7)	101	
TDA1387T	continuous calibration	DAC with current output		1	I^2S, up to $4f_S$	_88(0.004)	_35(1.7)	98	
TDA1312A(AT)[5]	continuous calibration	DAC with voltage output		1	“S”, up to $8f_S$	_68(0.04)	_33(2)	92	
TDA1311A(AT)[5]	continuous calibration	DAC with voltage output		1	“S”, up to $4f_S$	_68(0.04)	_33(2.2)	92	
TDA1310A(AT)	continuous calibration	DAC with current output		1	“S”, up to $4f_S$	_65(0.05)	_33(2.2)	95	

Notes: [1] measured with SAA7350 and 20-bit input; [2] includes digital filter; [3] high sound quality: dynamic
[4] A-weighting; [5] includes I/V converter.

	Type		Description	Over-sampling ($x f_S$)	Data input format	Typ. THD + N at 0 dB dB(%)	Typ
Bitstream/continuous calibration filter-DACs							
TDA1305T(AT)[2][6]	bitstream/CC filter-DAC			96	I^2S, “S”, $1f_S$, up to 20-bit	_90(0.003)	
TDA1546T[2]	bitstream/CC filter-DAC + DSP features			96	I^2S, “S”, $1f_S$, up to 20-bit	_88(0.004)	
TDA1548T[2]	low-voltage bitstream/CC filter-DAC + DSP features			96	I^2S, “S”, $1f_S$, up to 20-bit	_85(0.005)	
Continuous calibration filter-DACs							

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Table 2-3d Survey of stereo audio ADCs (ranked by typical THD + N at 0 dB performance per category)

	Type		Description	Over-sampling ($x f_S$)	Data input format	Typ. THD + N at 0 dB dB(%)	Typ
TDA1306T[2][6]	CC filter-DAC			4	I^2S, “S”, $1f_S$, up to 20-bit	_70(0.032)	
TDA1386T[2]	CC filter-DAC			4	I^2S, “S”, $1f_S$, up to 20-bit	_70(0.032)	
Quadruple sign-magnitude filter-DAC							
TDA1314T[5]	quad sign-magnitude filter-DAC with voltage output			4	2 x I^2S, $1f_S$, 18-bit with sign	_70(0.03)	

Notes: [1] measured with SAA7350 and 20-bit input; [2] includes digital filter; [3] high sound quality: dynamic
[4] A-weighting; [5] includes I/V converter.

	Type		Description	Over-sampling ($x f_S$)	Data input format	Typ. THD + N at 0 dB dB(%)	Typ. THD + N at dB(%) [4]	Typ
7366T	economy bitstream ADC			128	data output format: I^2S + one pseudo I^2S	_88(0.004)		
SAA7367T	economy bitstream ADC			128	data output format: I^2S + one pseudo I^2S	_88(0.004)		
SAA7360GP	high-performance bitstream ADC			128	data output format: I^2S + two pseudo I^2S	_90(0.003)		
SAA7361GP	premium-grade bitstream ADC			128	data output format: I^2S + two pseudo I^2S	_94(0.002)		

Notes: [1] measured with SAA7350 and 20-bit input; [2] includes digital filter; [3] high sound quality: dynamic
[4] A-weighting; [5] includes I/V converter.

dio ADCs + DACs

Type			Description	Over-sampling ($x f_S$)	Data input format	Typ. THD + N at 0 dB dB(%)	Typ. THD + N at dB(%) [4]	Typ. Signal-to-noise ratio (dB) [4]	Typical output voltage (or current) V (mA)	Supply voltage [6] (V)	Power
age bitstream/CC ADC + DAC		**ADC**		I^2S, “S”, 16-bit, 18-bit output	_85(0.005)	_85(1.7)	95		2.7 to 4.0	
		DAC	256	I^2S, “S”, 16-bit, 18-bit input	_90(0.003)	_44(0.6)	104	0.5		

Notes: [1] measured with SAA7350 and 20-bit input; [2] includes digital filter; [3] high sound quality: dynamic
[4] A-weighting; [5] includes I/V converter.

Table 2-4a Features of the high-performance bitstream digital filter

Type number	TDA1307
8-sample interpolation error concealment	_
Digital mute: attenuation _12 dB	_
8x oversampling Finite Impulse Response (FIR) filter; 39-bit	_
24x up-sampling	_
1-bit end quantization	_
Fade function; sophisticated volume control	_
Digital silence detection (output)	_
DC-cancelling filter (selectable)	_
Dedicated output to top-grade DAC TDA1547	_
Selectable 3rd/4th-order noise shaping	_
Simple 3-line serial microcontroller command interface	_
Peak detection (continuous) and readout to microcontroller	_
Digital de-emphasis (selectable, f_S conscious); 20-bit	_
Power-on reset	_
Standby function	_
Single or differential mode output configuration (selectable)	_
Selectable dither generation and automatic scaling	_
Flexible system clock oscillator circuitry	_
Digital audio output	32-bit words in bi-phase mark code
Input data format	I^2S, Sony 16/18/20-bit
Package	DIL42

Table 2-4b Features and performance of the top-grade BiMOS bitstream conversion DAC

Type number	TDA1547
Pulse density modulation	_
Inherently monotonic	_
No zero-crossing distortion	_
Typ. THD + N at full-scale (0 dB)dB(%)	_101 (0.0009)
Typ. signal-to-noise ratiodB	113
Dynamic rangedB	111
Channel separation at 1 kHzdB	115
Full-scale output voltage (RMS value)V	1.0
Package	DIL32

Table 2-4c Performance of TDA1307 with 4th-order noise shaper

Parameter	Value
Typ. dynamic rangedB	137
Typ. signal-to-noise ratiodB	142

TDA15
47

Table 2-5 Features and performance of the bitstream/continuous calibration DAC

Type number	TDA1549(T)
Simple application	_
Continuous calibration DAC combined with the bitstream technique	_
Cascaded 3-stage digital filter incorporating 7th-order half-band FIR filter stage, linear interpolator and sample and hold	_
Noise shaper	_
Single supply voltageV	3.4 to 5.5
x oversampling: normal speed mode ($f_{sys} = 256f_s$)	96
No zero crossing distortion	_
Typ. THD + N at full-scale (0 dB)dB(%)	_90(0.003)
Typ. THD + N at _60 dB (A-weighting)dB(%)	_50(0.32)
Typical signal-to-noise-ratio (A-weighting)dB	110
Serial input format	"S" $4f_s$, 18-bit
Full-scale output voltage (RMS value)V	1.5
Package	DIL16, SO16

Table 2-6 Features and performance of the high-performance 16-bit DACs

Type number	TDA1541A/S2	TDA1541A/S1	TDA1541A	TDA1541A/R 1
Dynamic Element Matching (DEM)	_	_	_	_
$4f_S$ or $8f_S$ oversampling	_	_	_	_
I^2S input data format, up to $8f_S$	_	_	_	_
TTL compatible inputs	_	_	_	_
Marked with single crown		_		
Marked with double crown	_			
Typ. THD + N at full-scale (0 dB)dB(%)	_97(0.002)	_95(0.001)	_95(0.0018)	_95(0.001)
Typ. THD + N at _60 dBdB(%)	_47(0.4)	_47(0.4)	_42(0.79)	_43(0.7)
Channel separationdB	98	98	98	98
Typ. signal-to-noise ratiodB	112	112	112	112
Full-scale output currentmA	4.0	4.0	4.0	4.0
Package	DIL28	DIL28	DIL28	DIL28

Table 2-7 Features and performance of the economy and low-noise 16-bit DACs

Type number	TDA1543(T)	TDA1543A(AT)
Economy DAC		_
Input format (time-division multiplexed, two's complement, TTL)	I^2S, up to $4f_S$	“S”, up to $4f_S$
Low distortion	_	_
16-bit dynamic range	_	_
Single 5 V power supply	_	_
4x oversampling possible	_	_
No peripheral components required	_	_
Adjustable bias current added to the output currents	_	_
Typ. THD + N at full-scale (0 dB)dB(%)	_75(0.01)	_75(0.01)
Typ. THD + N at _60 dB dB(%)	_33(2.2)	_33(2.2)
Typical signal-to-noise-ratio (A-weighting)dB	98	98
Full-scale output currentmA	2.30	2.30
Package	DIL8, SO16	DIL8, SO16

TDA1541
A
TDA1541
A/R1
TDA1541
A/S1
TDA1541/
S2

TDA1543(T
)
TDA1543A(
AT)

Table 2-8 Features and performance of CC-DACs with current output

Type number	TDA1310A(AT)	TDA1545A(AT)	TDA1387T
Low power consumption (6 mW with a 3 V supply)	–	–	–
Single 3 V to 5.5 V supply	–	–	–
Internal bias current ensures wide dynamic range (16-bit resolution)	–	–	–
Output current and bias current are proportional to the supply voltage	–	–	–
Short settling time permits $2f_s$, $4f_s$ or $8f_s$ oversampling (serial input) or double-speed operation at $4f_s$ oversampling	–	–	–
Input data format (time-division multiplexed, two's complement, TTL)	"S", up to $4f_s$	"S", up to $4f_s$	I^2S up to $4f_s$
No zero-crossing distortion	–	–	–
Operating temperature range°C	_40 to +85	_40 to +85	_40 to +85
Typ. THD + N at full-scale (0 dB)dB(%)	_65(0.05)	_88(0.004)	_88(0.004)
Typical signal-to-noise-ratio (A-weighting)dB	95	101	98
Full-scale output currentmA	1.0	1.0	1.0
Package	DIL8, SO8	DIL8, SO8	SO8

Table 2-9 Features and performance of CC-DACs with voltage output

Type number	TDA1311A(AT)	TDA1312A(AT)	TDA1313(T)
Internal bias current ensures wide dynamic range (16-bit resolution)	–	–	–
Output current and bias current are proportional to the supply voltage	–	–	–
Short settling time permits $2f_S$, $4f_S$ or $8f_S$ oversampling (serial input) or double-speed operation at $4f_S$ oversampling	–	–	–
Input data format (time-division multiplexed, two's complement, TTL)	"S", up to $4f_S$	"S", up to $8f_S$	"S", up to $4f_S$ (simultaneous) "S", up to $8f_S$ (parallel)
No zero-crossing distortion	_	_	_
Single supply voltageV	4 to 5.5	4 to 5.5	3 to 5.5
Power consumption with a 5 V supplymW	8	8	30
Operating temperature range˚C	_40 to +85	_40 to +85	_40 to +85
Typ. THD + N at full-scale (0 dB)dB(%)	_68(0.04)	_68(0.04)	_88(0.004)
Typ. THD + N at _60 dB (A-weighting)dB(%)	_33(2)	_33(2)	_38(1.3)
Typical signal-to-noise-ratio (A-weighting)dB	92	92	98
Full-scale output voltageV	2.0	2.0	4.2
Package	DIL8, SO8	DIL8, SO8	DIL16, SO16

TDA1311A(AT)
TDA1312A(AT)
TDA1313(T)

Table 2-10 Features and performance of the bitstream/continuous calibration filter-DACs

Type number	TDA1305T TDA1305AT	TDA1546T	TDA1548T
Simple application	_	_	_
Continuous calibration DAC combined with the bitstream technique	_	_	_
Cascaded 4-stage digital filter incorporating 2-stage FIR filter, linear interpolator and sample and hold	_	_	_
DSP features Digital volume and tone control		_	_
Master or slave mode clock system	_ (AT suffix) slave only (T suffix)	_	_
_12 dB fixed attenuation (volume control) via attenuation input control	_		
Smoothed transitions before and after muting (soft mute)	_	_	_
Noise shaper	_	_	_
Single supply voltageV	3.4 to 5.5	3.8 to 5.5	2.7 to 4
x oversampling: normal speed mode (f_{sys} = 256f_S) normal speed mode (f_{sys} = 384f_S) double speed mode (f_{sys} = 256f_S) double speed mode (f_{sys} = 384f_S)	 128 96 64 48	 128 96 64 48	 128 96 64 48
No zero crossing distortion	_	_	_
Typ. THD + N at full-scale (0 dB)dB(%)	_90(0.003)	_88(0.004)	_85(.0056)
Typ. THD + N at _60 dB (A-weighting)dB(%)	_46(0.5)	_44(0.6)	_35(1.179)
Typical signal-to-noise-ratio (A-weighting)dB	110	108	95
Digital de-emphasis filter for 3 sampling rates kHz	32, 44.1, 48	All	44.1
Serial input format	I^2S, “S” 1f_S, 16, 18 or 20-bit	I^2S, “S” 1f_S, 16, 18 or 20-bit	I^2S, “S” 1f_S, 16, 18 or 20-bit
Full-scale output voltage (RMS value)V	1.5	1.5	0.7
Selectable system clockx f_S	256, 384	256, 384	256, 384, 64
Package	SO28	SO28	SO28

TDA13
05T
TDA13
05AT

TDA15
46T


TDA15
48T

Table 2-11 Features and performance of the continuous calibration filter-DACs

Type number	TDA1306T	TDA1386T
Simple application	_	_
Continuous calibration DAC combined with the bitstream technique	_	_
Cascaded 4-stage digital filter incorporating IIR filter stage	_	_
_12 dB fixed attenuation (volume control) via attenuation input control	_	_
Smoothed transitions before and after muting (soft mute)	_	_
Variable volume control via microcontroller interface	_	_
Noise shaper	_	_
Single supply voltageV	4.5 to 5.5	4.5 to 5.5
x oversampling:		
normal speed mode (f_{sys} = 256f_S)	4	4
normal speed mode (f_{sys} = 384f_S)	4	4
double speed mode (f_{sys} = 256f_S)	2	2
double speed mode (f_{sys} = 384f_S)	2	2
No zero crossing distortion	_	_
Typ. THD + N at full-scale (0 dB)dB(%)	_70(0.032)	_70(0.032)
Typ. THD + N at _60 dB (A-weighting)dB(%)	_42(0.8)	_42(0.8)
Typical signal-to-noise-ratio (A-weighting)dB	110	108
Digital de-emphasis filter for 3 sampling rates kHz	44.1	44.1
Serial input format	I^2S, “S” 1f_S, 16, 18 or 20-bit	I^2S, “S” 1f_S, 16, 18 or 20-bit
Full-scale output voltage (RMS value)V	1.1	1.1
Selectable system clockx f_S	256, 384	256, 384
Package	SO24	SO24

Table 2-12 Features and performance of the quadruple sign-magnitude filter-DAC

Type number	TDA1314T
Wide dynamic range (102 dB typical) allows digital (DSP) volume control	_
Four times bit-serial oversampling filter	_
First-order $4f_s$ noise shaper	_
Four (front + rear stereo) very-low-noise sign-magnitude DACs for car digital audio applications	_
Only 1st-order post filtering required	_
Smooth power-on of the DAC output currents	_
Automatic digital PLL divider range setting allows the master clock to be selected over a wide range	_
Jitter on the I^2S signals does not degrade the THD	_
Single supply voltageV	4.75 to 5.25
Typ. power dissipationmW	85
Resolution of the DACs (length of data input words)bits	18
Typ. THD + N at full-scale (0 dB)dB(%)	_70(0.03)
Typ. Digital silence (no signal, A-weighted)dBA	_110
Serial input format	2 x I^2S, $1f_s$, 18-bit with sign
Output voltage range (5 kΩ load, 3 kΩ feedback)V_{RMS}	1
Typ. full-scale output current (R_{ref} = 20.5 kΩ)mA	0.5
Operating ambient temperature range°C	_40 to +85
Package	SO28

Table 2-13 Features and performance of the bitstream conversion ADCs

Type number	SAA7360GP	SAA7361GP	SAA7366T	SAA7367GP
Stereo, single-ended inputs	_	_	_	_
Input buffer for filtering and pre-scaling	_	_	_	
Fully differential ADC using 3rd-order Sigma-Delta modulation	_	_	_	_
x 128 oversampling, 4-stage decimation filter	_	_	_	_
Switchable high-pass filter to remove DC offsets	_	_	_	_
16- or 18-bit selectable output in I^2S and two pseudo I^2S formats	_	_		
18-bit output in I^2S and one pseudo I^2S format			_	_
Master or slave operation	_	_	_	slave mode
Single power supply (V_{DD})V	5 ±10%	5 ±10%	5 ±10%	5 ±10%
Power supply of 3.4 V to 5.5 V for the digital section			_	_
Crystal frequencyx f_s	256 or 512	256 or 512	256	256
Sampling ratekHz	18 to 53	18 to 53	18 to 53	18 to 53
Anti-aliasing suppressiondB	>_93	>_93	>_60	>_60
In-band rippledB	<0.0002	<0.0002	<±0.1	<±0.1
Min. dynamic rangedB	93	93	90	90
Max. THD + N at _1 dB digital outputdB(%)	_85 (0.005)	_90 (0.003)	_80 (0.01)	_80 (0.01)
Analog input voltageV	V_{DD}/2 ±5%	V_{DD}/2 nom.	V_{DD}/2 ±5%	V_{DD}/2 ±5%
Package	QFP44	QFP44	SO24	SO16

Table 2-14 Features and performance of the low-voltage bitstream/CC ADC + DAC

Type number	TDA1309H
Low supply voltage and power consumption allow use in portable equipment	_
Integrated high-pass filter to cancel DC offset (ADCs)	_
Analog loop-through function with power-down of unused digital circuitry	_
$256f_S$ system clock frequency in ADC and DAC mode	_
Choice of three system clock frequencies ($192f_S$, $256f_S$ and $384f_S$,) in DAC mode	_
Only 1st-order (one external capacitor) filtering required for DACs	_
Several power-down modes; separate power-down modes for ADCs and DACs	_
Digital de-emphasis (DACs)	_
Input pads suitable for 5.5 V/low-voltage interfacing	_
Wide dynamic range	_
Over-samplingx f_S	256 (DAC)
Data format at DAC input/ADC output	I^2S, “S”, 16-bit, 18-bit
Typical THD + N at 0 dB for ADCdB (%)	_85 (0.005)
Typical THD + N at 0 dB for DACdB (%)	_90 (0.003)
Maximum THD + N at 0 dB for ADCdB (%)	_80 (0.01)
Maximum THD + N at 0 dB for DACdB (%)	_82 (0.08)
Typical THD + N at _60 dB for ADCdB (%)	_35 (1.7)
Typical THD + N at _60 dB for DACdB (%)	_44 (0.6)
Typical signal-to-noise ratio for ADC (A-weighting)dB	99
Typical signal-to-noise ratio for DAC (A-weighting)dB	104
Single supply voltageV	2.7 to 4.0
Power dissipationmW	72 (ADC) 84 (DAC)
Operating ambient temperature range˚C	_40 to +85
Package	QFP44SL

SECTION 3 - DEDICATED SIGNAL PROCESSING ICs

Digital audio input/output (DAIO) circuit (Table 3-2)

This is a completely integrated CMOS transceiver for biphase-mark encoded digital audio signals that conform to the SPDIF (Sony Philips Digital Interface) and IEC958 interface standards (consumer mode).

In the receiver mode, the IC adjusts automatically to one of the three standardized sample frequencies (32 kHz for digital satellite signals, 44.1 kHz for compact disc signals, or 48 kHz for digital audio tape signals), decodes the input signal, and separates the audio and control data. A clock signal of $256f_S$ or $384f_S$ is generated to serve as a master clock signal for the digital audio system.

In the transmitter mode, the IC multiplexes the audio, control and user data and encodes them for subsequent transmission via a cable or optical link.

General Digital Input (GDIN) circuit (Table 3-3)

In the SRC (Sample Rate Conversion) mode, this very versatile IC can perform high-quality sample rate conversion of digital audio signals. I reads several serial input formats and includes a Audio Digital Input Circuit (ADIC) for input signals in the IEC958 format (also known as AES/EBU or SPDIF signals). An internal PLL removes excessive jitter from the incoming digital audio signals without the need for analog loop electronics. In-audio-band noise shaping can limit the standard 20-bit output word to 16 or 18 bits.

In the AD/DA mode, the on-chip digital filters can be used for bitstream A/D and D/A conversion.

In the slave-VCO and slave-VCXO modes. the internal PLL can be reconfigured to operate in a slave mode wherein the IC is locked to the incoming sampling rate.

Digital Audio Processing IC (DAPIC) (Table 3-4)

This is a very flexible function-specific 4-channel digital signal processor (DSP) for audio signals. In the general DAPIC mode, it can provide listening environment enhancements such as equalization, concert hall-effects, reverberation, surround sound/karaoke processing, and digital volume/balance control.

In the dual/quad filter modes, the IC can also be reconfigured as a dual or quad digital filter with programmable frequency characteristics.

A stereo expansion mode provides stereo digital filtering, 5-band graphic equalization and complex stereo expansion for headphone out-of-head and incredible stereo applications.

Function parameters, correction coefficients and a number of configurations can be downloaded to the IC via an I^2C-bus interface.

Headphone driver for digital audio (Table 3-5)

This is a high-performance stereo class AB headphone driver. Fabrication with a 1 µm CMOS process and assembly in an 8-pin surface-mounting package gives this IC the low power consumption and small size which is vital for battery-powered portable digital audio applications.

Dolby Pro Logic surround sound circuit (Table 3-6)

This is a high-quality audio-performance add-on digital signal processor. It comprises all the necessary features on chip for complete Dolby Surround Pro Logic sound.

In addition, the device also incorporates 3- and 5-band parametric equalizers, and tone and volume controls. These features can be used to replicate surround sound as an alternative to Dolby Pro Logic, or when the input is non-Dolby surround coded.

MPEG devices (Tables 3-7 and 3-8)

The perceptual audio encoding/decoding scheme defined within the ISO/IEC MPEG-1 (Motion Picture Expert Group) Audio Standard (11172-3) results in considerable reduction of the quantity of data required for digital audio, yet maintains a high level of perceived sound quality. The coding is based on a psycho-acoustic model of the human auditory system and exploits the fact that weak spectral components are inaudible if they are in the proximity (in both time and frequency) of loud components. This phenomenon is called masking.

Layers I and II of ISO/MPEG-1 reduce the data by splitting the broadband audio source signal into 32 sub-bands of equal width. The masking threshold (the amount of imperceptible audio energy as a function of frequency) is determined for the given signal by using the psycho-acoustic model. The sub-band samples are then re-quantized to an accuracy

that ensures that the spectral distribution of the re-quantization noise does not exceed the

masking threshold. This reduction of representation accuracy provides the reduction of the audio data. The re-quantized sub-band samples are multiplexed with side information concerning the actual re-quantization to form the MPEG audio bitstream.

During decoding, the MPEG audio bitstream is de-multiplexed and the side information is used to reconstruct the sub-band signals which are combined to form a broadband audio output signal.

We have the following family of MPEG ICs.

Stereo filter/CODEC for an MPEG-1 Layer I decoder

An MPEG-1 Layer I decoder can be implemented by using the stereo filter/CODEC SAA2520GP together with a digital audio input/output (DAIO) circuit TDA1315H and a stereo DAC as shown in Fig.3-1.

Masking threshold processor for an MPEG-1 Layer I encoder

An MPEG-1 Layer I encoder can be implemented by using the masking threshold processor SAA2521 with a stereo filter/CODEC SAA2520GP, a digital audio input/output (DAIO) circuit TDA1315H, and a stereo ADC as shown in Fig.3-2.

ISO/MPEG audio source decoder for an MPEG-1 decoder for Layers I and II

An MPEG-1 decoder for Layers I and II can be implemented by using the ISO/MPEG audio source decoder SAA2500H with a DAC as shown in Fig.3-3.

Digital audio broadcast decoder

This IC (SAA2501H) is suitable for audio broadcast applications and complies with Eureka-147.

MPEG-1/2-compatible audio decoder

This highly-featured decoder SAA2502H is optimized for use with MPEG 2 video decoders in digital multimedia systems.

Table 3-1 Documentation relating to dedicated signal processing ICs

Title	Ordering code	Type of publication
Outline of a layer-1 MPEG decoder using the SAA2520	SAU/AN92012	Application note

Table 3-2 Features and performance of the digital audio input/output (DAIO) circuit

	Type number: TDA1315H
Transceiver for SPDIF and IEC958 encoded signals	_
Highly sensitive input for transformer-coupled links	_
TTL level input for optical links	_
Built-in IEC input selector	_
Built-in IEC feed-through function	_
Automatic sample frequency detection	_
System clock recovery from input signal	_
Error detection and concealment	_
PLL lock detection in transmit mode	_
Serial audio interface conforms to I^2S format	_
Auxiliary I^2S input for ADC	_
Audio output selector	_
Microprocessor-controlled and stand-alone modes	_
128-byte buffer for user data	_
Bytewise exchange of user data with microprocessor	_
Decoding of compact disc subcode Q-channel data	_
Support for Serial Copy Management System (SCMS)	_
LED drive capability (sample frequency and error indication)	_
Pin-selectable device address for microprocessor interface	_
Supply voltage rangeV	3.4 to 5.5
Operating temperature range˚C	_40 to +85
Package	SQFP44

MPEG layer-1 audio compression/decompression chip-set	SAU/AN92013	Application note
Design of 8 kHz-LP and 4 kHz-LP measurement filters	AT-AU18/89	Application note
Advance information on the Philips SAA2500 ISO/MPEG audio source decoder	SAU/AN93008	Application note
User guide for the Philips SAA2520/SAA2521 MPEG audio layer 1 demonstration unit	SAU/AN93016	Application note
SAA7274 Audio Digital Input Circuit for converting SPDIF signals into I^2S signals	NBA/AN9102	Application note
TDA1315 Digital Audio Input/Output circuit	NBA/AN9309	Application note

TDA13
15H

Table 3-3 Features and performance of the general digital input (GDIN) circuit

Type number	TDA1373H
Fabricated in 1.0 µm double-metal CMOS	_
Four operating modes (SRC, AD/DA, SLAVE-VCO, SLAVE-VCXO)	_
Full digital sampling rate conversion (SRC) over a wide range of input sampling rates	_
Fast and automatic detection and locking to the input sampling rate with continuous tracking	_
Digital PLL with adaptive bandwidth which removes jitter on the digital audio input	_
Audio outputs soft muted during loop acquisition	_
Full linear-phase processing based on all-FIR filtering	_
On-chip fully-digital IEC958 demodulator for digital input signals (AES/EBU or SPDIF format)	_
Extended input sampling frequency range	_
IEC958 Channel Status (CS) and User Channel (UC) outputs	_
On-chip CS and/or UC demodulation and buffering (consumer and professional format)	_
Dedicated sub-code processing for CD	_
Final output quantization to 16/18/20 bits with optional in-audio-band noise shaping	_
Bitstream input and output for coupling to 1-bit ADC and DAC	_
I^2S and Japanese serial input formats supported for SRC and DAC functions	_
I^2S and Japanese serial output formats supported for SRC and ADC functions	_
I^2S and Japanese 4x oversampled serial output available for SRC and ADC functions	_
8-bit digital gain/attenuation control	_
Switchable DSP interface (I^2S input and output) for additional audio processing	_
Additional clock outputs available at 768, 384, 256 and 128$f_{s\ out}$	_
3-line serial microcontroller interface compatible with Philips CD I.C. protocol (HCL)	_
SRC THD + N over the 0 to 20 kHz band (1 kHz, 20 bits input and output)dB	_113
SRC THD + N over the 0 to 20 kHz band (1 kHz, 16 bits input and output)dB	_95
Pass-band ripple for up-sampling and down-sampling filtersdB	>±0.004
Selectable stop-band suppression for 64x up-sampling filtersdB	70 to 50
Stop-band suppression for 128x down-sampling filtersdB	80
Maximum output sample frequencykHz	55
AC input voltage at IEC input (DIIS)V_{p-p}	0.2
Supply voltage range ($f_{s\ out}$ = 44.1 kHz)V	4.75 to 5.5
Total supply current ($f_{s\ out}$ = 44.1 kHz)mA	166
Total power dissipation ($f_{s\ out}$ = 44.1 kHz)mW	830
Operating temperature range°C	0 to +70
Package	QFP64

Table 3-4 Features and performance of the digital audio processing IC (DAPIC)

Type number	SAA7740H
Hardware features	
Two digital audio inputs in the I^2S format (four audio channels)	_
Two digital audio outputs in the I^2S format (four audio channels)	_
Independent input and output interfaces	_
Slave input and output interfaces	_
Slave processing	_
I^2C microcontroller interface	_
DC filtering at the inputs	_
One programmable 2nd-order digital filter unit	_
Two MAC units (24*16 bits/MAC)	_
DRAM interface and address computation unit for external delay lines	_
On-chip coefficient and external delay-line address storage	_
Hard-controlled soft mute via the MUTE pin	_
Hard-controlled soft de-mute via the RESET pin	_
Software features	
5-band parametric equalizer with selectable centre freq., slope and boost/cut gain settings of ±12 dB	_
Stereo width control from mono to stereo to spatial stereo	_
Stereo listening environment acoustic effects (e.g. concert hall) with 8 coefficients and 8 delayed taps per channel	_
External delay-line processing for delays of up to 1 s	_
Reverberation with selectable reverberation time (up to 5 s) and energy	_
Three different surround sound programs to obtain a spatial effect with four loudspeakers	_
Passive Dolby surround sound processing, with addition of an external dynamic noise reduction IC	_
Karaoke processing	_
Dual 16th-order correction filtering	_
Quad 8th-order correction filtering	_
Digital volume and balance control	_
Soft-controlled soft mute/de-mute via the microcontroller interface	_
Input switching matrix	_
Output front and rear switching matrix	_
Characteristics	
Typical crystal frequencyMHz	16.9344
Supply voltage range V	4.5 to 5.5
Total supply current (f_C = 16.9344 Mhz)mA	145
Total power dissipation (f_C = 16.9344 Mhz)mW	700
Operating temperature range°C	_40 to +85
Package	QFP64

SAA77
40H

Table 3-5 Features and performance of the class-AB stereo headphone driver for digital audio

Type number	TDA1308T
Large output voltage swing	_
No switch-on/switch-off clicks	_
Excellent power supply ripple rejection	_
Output short-circuit proof	_
CMOS technology for low power consumption	_
High performance; high S/N ratio, high slew rate, low distortion	_
Single supply voltageV	3 to 7
Dual supply voltageV	±1.5 to ±3.5
Typical supply currentmA	3
Typical power dissipationmW	15
Maximum output power (THD <0.1%)mW	60
Typical THD + N at 0 dBdB (%)	_70 (0.03)
Typical signal-to-noise ratiodB	110
Typical channel separationdB	70
Typical power supply ripple rejection ratio (f = 100 Hz, V_{ripple} = 100 mV_{p-p})dB	90
Operating temperature range°C	_40 to +85
Package	SO8

Table 3-6 Features and performance of the Dolby Pro Logic surround sound IC

Type number	SAA7710T
Adaptive matrix	_
7 kHz low-pass filters	_
Adjustable delay for surround channel	_
Modified Dolby B noise reduction	_
Noise sequencer	_
Output volume control	_
Automatic balance and master level control with DC-offset filter	_
Hall and matrix surround sound functions	_
Either: _ 3-band parametric equalizer on main channels left, centre, right (f_S = 44.1 kHz), or _ 5-band parametric equalizer on main channels left, centre, right (f_S = 32 kHz), or _ tone control (bass/treble) on all four output channels (f_S = 44.1 kHz)	_
Optional clock divider for crystal oscillator	_
I^2C-bus mode control	_
Centre mode control	ON/OFF, normal, phantom, wide
Stereo I^2C digital input channels	2
Stereo I^2C digital output channels	2
4-channel active surround soundHz	20 to 20 000
On-chip delay line (f_S =44.1 kHz)ms	≤45
Supply voltageV	4.5 to 5.5
Package	SO32

TDA13
08T

SAA77
10T

Table 3-7 Features and performance of the MPEG-1 Layer I ICs

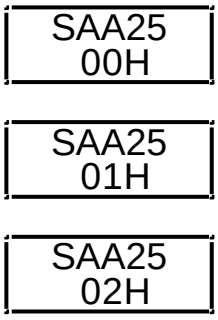
Type number	SAA2520GP	SAA2521GP
Stereo filter/CODEC	_	
Masking threshold processor		_
ISO/MPEG audio source decoder		
Layer I compatible	_	_
Layer I and Layer II compatible		
Microcontroller interface	_	_
Low power consumption	_	_
I^2S interface	_	_
Clock generator	_	
Required for Layer I encoding	_	_
Options for Layer I decoding	_	
Layer I and Layer II decoding		
Microcontrolled and stand-alone modes	_	
Error concealment		
Burst mode data input		
Stereo	_	_
Sample clock switching	_	_
Variable bit precision	_	_
Supply voltageV	3.8 to 5.5	3.8 to 5.5
Operating temperature range°C	_40 to +85	_40 to +85
Package	QFP44	QFP44


SAA252
0GP


SAA252
1GP

Table 3-8 Features and performance of the MPEG-1 Layers I and II ICs

Type number	SAA2500H	SAA2501H	SAA2502H
ISO/MPEG audio source decoder	_	_	_
Layer I and Layer II compatible	_	_	_
Suitable for DAB (Eureka-147 compatible)		_	
Decoded sub-band signal output for concealment		_	
Processing of programme and audio service synchronized data		_	
Dynamic range control			_
MPEG 2 compatible (for stereo output)			_
Handles byte- and non-byte-aligned input data			_
I^2C microcontroller interface			_
IEC 958 digital output			_
Integrated DAC			_
256 x f_S clock locked to external reference			_
I^2S interface	_	_	_
Low power consumption	_	_	_
L3 microcontroller interface	_	_	_
Clock generator	_	_	_
Microcontrolled and stand-alone modes	_	_	_
Error concealment	_	_	_
Burst mode data input	_	_	_
Stereo	_	_	_
Sample clock switching	_	_	_
Variable bit precision	_	_	_
Supply voltageV	5 ±10%	5 ±10%	5 ±10%
Package	QFP44	QFP44	QFP44


SAA25
00H
SAA25
01H
SAA25
02H

SECTION 4 - INDEX OF AUDIO DATA CONVERTERS AND DEDICATED SIGNAL PROCESSING ICs